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EXAMINER	
LEWIS, MONICA	

ART UNIT	PAPER NUMBER
2822	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/801,475	CHEN ET AL.	
	Examiner	Art Unit	
	Monica Lewis	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 June 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14,19 and 20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13,19 and 20* is/are rejected.

7)☒ Claim(s) *14* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to the response filed on June 29, 2007.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1, 2, 6, 7, 9 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee (U.S. Patent No. 5,905,289) in view of Tomita et al. (U.S. Publication No. 2005/0035457).

In regards to claim 1, Lee discloses the following:

a) a semiconductor substrate (10) (For Example: See Figure 12);

b) one or more metallurgy layers connected to the semiconductor substrate, wherein each of the one or more metallurgy layers comprises one or more conductive lines (20 and 22) and one or more dummy structures (44) between the one or more conductive lines (For Example: See Figure 12); and

c) one or more dielectric layers (48 and 46) between the one or more metallurgy layers (For Example: See Figure 12).

In regards to claim 1, Lee fails to disclose the following:

a) dummy structures from different metallurgy layers are thermally connected.

However, Tomita et al. ("Tomita") discloses a semiconductor device that has dummy structures (29a and 15a) from different metallurgy layers that are thermally connected (28c) (For Example: See Figure 7). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor of Lee to include a semiconductor device that has dummy structures from different metallurgy layers that are thermally connected

as disclosed in Lin because it aids in protecting against external noise (For Example: See Paragraph 8).

Additionally, since Lee and Tomita are both from the same field of endeavor, the purpose disclosed by Tomita would have been recognized in the pertinent art of Lee.

In regards to claim 2, Lee fails to disclose the following:

a) there are at least two of the metallurgy layers that each include at least two of the dummy structures and wherein at least two of the dummy structures on a first metallurgy layer are connected to at least two of the dummy structures on a second metallurgy layers through a plurality of vias.

However, Tomita discloses a semiconductor device that has dummy structures (29a) on a first metallurgy layer are connected to at least the dummy structures (15a) on a second metallurgy layer through a plurality of vias (28c) (For Example: See Figure 7). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor of Lee to include a semiconductor device that has dummy structures from different metallurgy layers that are connected through vias as disclosed in Lin because it aids in protecting against external noise (For Example: See Paragraph 8).

Additionally, since Lee and Tomita are both from the same field of endeavor, the purpose disclosed by Tomita would have been recognized in the pertinent art of Lee.

In regards to claim 6, Lee discloses the following:

a) the width of one of the one or more dummy structures is substantially the same as the width of the one or more conductive lines (For Example: See Figure 12).

In regards to claim 7, Lee fails to disclose the following:

a) at least two of the two dummy comprise different shapes.

However, Tomita discloses a semiconductor device where two dummy structures comprise different shapes (For Example: See Figure 6). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor of Lee to include a semiconductor device where two dummy structures comprise different shapes as disclosed in Lin because it aids in protecting against external noise (For Example: See Paragraph 8).

Additionally, since Lee and Tomita are both from the same field of endeavor, the purpose disclosed by Tomita would have been recognized in the pertinent art of Lee.

In regards to claim 9, Lee fails to disclose the following:

a) at least two of the dummy structures comprise different sizes.

However, Tomita discloses a semiconductor device where two dummy structures comprise different sizes (For Example: See Figure 6). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor of Lee to include a semiconductor device where two dummy structures comprise different sizes as disclosed in Lin because it aids in protecting against external noise (For Example: See Paragraph 8).

Additionally, since Lee and Tomita are both from the same field of endeavor, the purpose disclosed by Tomita would have been recognized in the pertinent art of Lee.

In regards to claim 10, Lee fails to disclose the following:

a) there are at least two of the dummy structures that are connected by a first line, wherein the width of the first line is less than the width of each of the two dummy structures.

However, Tomita discloses a semiconductor device where two dummy structures are connected by a first line, wherein the width of the first line is less than the width of each of the

two dummy structures (For Example: See Figure 7). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor of Lee to include a semiconductor device where two dummy structures are connected by a first line, wherein the width of the first line is less than the width of each of the two dummy structures as disclosed in Lin because it aids in protecting against external noise (For Example: See Paragraph 8).

Additionally, since Lee and Tomita are both from the same field of endeavor, the purpose disclosed by Tomita would have been recognized in the pertinent art of Lee.

4. Claims 3, 4 and 11-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee (U.S. Patent No. 5,905,289) in view of Tomita et al. (U.S. Publication No. 2005/0035457) and *Microchip Fabrication* by Peter Van Zant.

In regards to claim 3, Lee fails to disclose the following:

a) at least one or more dummy structure comprises copper.

However, Van Zant discloses the use of copper (For Example: See Pages 400-401). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor of Lee to include the use of copper as disclosed in Van Zant because it is a better conductor (For Example: See Page 401).

Additionally, since Lee and Van Zant are both from the same field of endeavor, the purpose disclosed by Van Zant would have been recognized in the pertinent art of Lee.

In regards to claim 4, Lee fails to disclose the following:

a) at least one or more dummy structure comprises aluminum.

However, Van Zant discloses the use of aluminum (For Example: See Pages 398-399). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor of Lee to include the use of aluminum as disclosed in Van Zant because it aids in providing low resistivity (For Example: See Pages 398-399).

Additionally, since Lee and Van Zant are both from the same field of endeavor, the purpose disclosed by Van Zant would have been recognized in the pertinent art of Lee.

In regards to claim 11, Lee fails to disclose the following:

a) the first line comprises copper.

However, Van Zant discloses the use of copper (For Example: See Pages 400-401). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor of Lee to include the use of copper as disclosed in Van Zant because it is a better conductor (For Example: See Page 401).

Additionally, since Lee and Van Zant are both from the same field of endeavor, the purpose disclosed by Van Zant would have been recognized in the pertinent art of Lee.

In regards to claim 12, Lee fails to disclose the following:

a) the first line comprises aluminum.

However, Van Zant discloses the use of aluminum (For Example: See Pages 398-399). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor of Lee to include the use of aluminum as disclosed in Van Zant because it aids in providing low resistivity (For Example: See Pages 398-399).

Additionally, since Lee and Van Zant are both from the same field of endeavor, the purpose disclosed by Van Zant would have been recognized in the pertinent art of Lee.

In regards to claim 13, Lee fails to disclose the following:

a) another two dummy structures are connected by a second line, wherein the first lien and the second line comprise identical materials.

However, Tomita discloses a semiconductor device that has another two dummy structures that are connected by a second line, wherein the first lien and the second line comprise identical materials (For Example: See Figure 6). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor of Lee to include a semiconductor device that has another two dummy structures are connected by a second line, wherein the first lien and the second line comprise identical materials as disclosed in Tomita because it aids in protecting against external noise (For Example: See Paragraph 8).

Additionally, since Lee and Tomita are both from the same field of endeavor, the purpose disclosed by Tomita would have been recognized in the pertinent art of Lee.

5. Claims 5, 19 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee (U.S. Patent No. 5,905,289) in view of Tomita et al. (U.S. Publication No. 2005/0035457) and Iguchi (U.S. Patent No. 6,225,697).

In regards to claim 5, Lee fails to disclose the following:

a) the distance between one the dummy structures and one of the one or more conductive lines is at least .1 um.

However, Iguchi discloses the distance between one the dummy structures and one of the one or more conductive lines is at least .1 um (For Example: See Figure 1 and Column 7 Lines 23-33). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor of Lee to include that the distance between one

the dummy structures and one of the one or more conductive lines is at least .1 um as disclosed in Iguchi because it aids in reducing wire capacitance (For Example: See Column 7 Lines 23-33).

Additionally, since Lee and Iguchi are both from the same field of endeavor, the purpose disclosed by Iguchi would have been recognized in the pertinent art of Lee.

In regards to claim 19, Lee discloses the following:

a) a semiconductor substrate (For Example: See Figure 12);

b) one or more metallurgy layers connected to the semiconductor substrate wherein each of the one or more metallurgy layers comprises one or more conductive lines and one or more dummy structures between the one or more conductive lines (For Example: See Figure 12); and

c) one or more dielectric layers between the one or more metallurgy layers (For Example: See Figure 12).

In regards to claim 19, Lee fails to disclose the following:

a) the distance between one the dummy structures and one of the one or more conductive lines is at least .1 um.

However, Iguchi discloses the distance between one the dummy structures and one of the one or more conductive lines is at least .1 um (For Example: See Figure 1 and Column 7 Lines 23-33). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor of Lee to include that the distance between one the dummy structures and one of the one or more conductive lines is at least .1 um as disclosed in Iguchi because it aids in reducing wire capacitance (For Example: See Column 7 Lines 23-33).

Additionally, since Lee and Iguchi are both from the same field of endeavor, the purpose disclosed by Iguchi would have been recognized in the pertinent art of Lee.

b) wherein at least two of the dummy structures on a first metallurgy layer are connected to at least two of the dummy structures on a second metallurgy layers through a plurality of vias.

However, Tomita discloses a semiconductor device that has dummy structures on a first metallurgy layer are connected to at least the dummy structures on a second metallurgy layer through a plurality of vias (For Example: See Figure 7). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor of Lee to include a semiconductor device that has dummy structures from different metallurgy layers that are connected through vias as disclosed in Lin because it aids in protecting against external noise (For Example: See Paragraph 8).

Additionally, since Lee and Tomita are both from the same field of endeavor, the purpose disclosed by Tomita would have been recognized in the pertinent art of Lee.

c) the dummy metal structures are connected by metal lines.

However, Tomita discloses a semiconductor device that has dummy structures connected by metal lines (For Example: See Figure 4). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor of Lee to include a semiconductor device that has dummy structures connected by metal lines as disclosed in Lin because it aids in providing a connection among the components (For Example: See Figure 4).

Additionally, since Lee and Tomita are both from the same field of endeavor, the purpose disclosed by Tomita would have been recognized in the pertinent art of Lee.

In regards to claim 20, Lee discloses the following:

a) the respective heights of the metal lines and the dummy metal structures are similar (For Example: See Figure 12).

6. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lee (U.S. Patent No. 5,905,289) in view of Tomita et al. (U.S. Publication No. 2005/0035457) and Landis (U.S. Publication No. 2004/0195670).

In regards to claim 8, Lee fails to disclose the following:

a) the two dummy structures comprise different materials.

However, Landis discloses two dummy structures (35 and 50) that comprise different materials (For Example: See Paragraphs 24 and 25). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor of Lee to include two dummy structures that comprise different materials as disclosed in Landis because it aids in reducing deflections (For Example: See Paragraph 3).

Additionally, since Lee and Landis are both from the same field of endeavor, the purpose disclosed by Landis would have been recognized in the pertinent art of Lee.

Allowable Subject Matter

7. Claim 14 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

8. Applicant's arguments filed 6/29/07 have been fully considered but they are not persuasive. First, Applicant argues that the "Tomita's focus is (1) inhibiting the occurrence of resist poisoning and (2) providing protection against external electromagnetic noise...heat and thermal do not appear anywhere within Tomita much less in association with dummy structure." As previously stated, the fact that applicant has recognized another advantage which would flow

naturally from following the suggestion of the prior art cannot be the basis for patentability when the differences would otherwise be obvious. See *Ex parte Obiaya*, 227 USPQ 58, 60 (Bd. Pat. App. & Inter. 1985). The fact that a reference does not disclose a particular word does not mean that the limitations are not disclosed. Tomita discloses a semiconductor device that has dummy structures (29a and 15a) from different metallurgy layers that are thermally connected (28c) (For Example: See Figure 7).

Second, Applicant argued that "the Obiaya decision had absolutely nothing to do with the issue of whether or not a particular reference constitutes analogous prior art." However, Obiaya was not utilized for analogous art. Obiaya was utilized to disclose a different reason for combining.

Third, Applicant argues that "the Examiner asserts that Oetiker supports the Examiner's position that Lee and Tomita are analogous prior art...Oetiker does not support the Examiner's position...the Examiner further asserts that semiconductors is a field of endeavor, and that everything relating to semiconductors is within this field....the particular problem with which the Applicants were concerned...is heat dissipation...neither Lee nor Tomita has any teachings about heat dissipation." However, as previously stated, it has been held that a prior art reference must either be in the field of applicant's endeavor or, if not, then be reasonably pertinent to the particular problem with which the applicant was concerned, in order to be relied upon as a basis for rejection of the claimed invention. See *In re Oetiker*, 977 F.2d 1443, 24 USPQ2d 1443 (Fed. Cir. 1992). In this case, they are both from the same field of endeavor (semiconductors). Additionally, as previously stated, the fact that a reference does not disclose a particular word does not mean that the limitations are not disclosed.

Finally, Applicant argues that the "the idea to modify Lee in view of Tomita is not coming from what was known before the present invention, but instead is necessarily coming from hindsight of Applicant's disclosure." In response to applicant's argument that the examiner's conclusion of obviousness is based upon improper hindsight reasoning, it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971).

Conclusion

9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Monica Lewis whose telephone number is 571-272-1838. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith can be reached on 571-272-2429. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300 for regular and after final communications.

ML

September 11, 2007

MONICA LEWIS
PRIMARY PATENT EXAMINER